CIO-DIO24
CIO-DIO24H
CIO-DIO24/CTR3

User's Manual

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1 INTRODUCTION

This manual provides information on the CIO-DIO24, CIO-DIO24H and CIO-DIO24/CTR3 digital I/O boards and accessories. The manual is organized into separate sections for those aspects of a product which are unique. Some issues, such as simple programming and electronic interfacing are applicable to all of the digital boards.

The CIO-DIO24 has a single 82C55 digital I/ O chip interfaced to the PC bus, with all its I/O lines accessible through the board's 37-pin connector. The I/O pins of an 82C55 are CMOS TTL level.

CIO-DIO24H is a high-drive TTL, 24-line digital I/O board. The control register which sets the direction of the I/O ports is identical to an 82C55 in mode 0 (see 82C55 data sheet). The outputs are capable of sourcing 15 mA and sinking 64 mA.

CIO-DIO24/CTR3 is a CIO-DIO24 with an 82C54 counter added. The 82C54 chip has three, 16-bit down-counters. The 82C54 Clock Inputs, Gates and Outputs are brought out to those pins which were used for bus power access on the CIO-DIO24 and CIO-DIO24H. The first counter (0) can be clocked from an internal 10 MHz crystal oscillator or an external clock source. The CIO-DIO24/CTR3 uses eight I/O addresses. The lower four are used by the 82C55 digital I/O chip and the upper four are used by the 82C54 counter/timer.

All these boards have the same connector pinout and respond to the same software instructions except for the CIO-DIO24/CTR3 counter signals.

This manual provides information on programming the 82C55 in mode 0. Those wishing to use the 82C55 in modes 1 or 2, or who wish to program the 82C54 counter on the CIO-DIO24/CTR3, must procure a data book from Intel Corporation Literature Department.

All of these products are supported by the Universal Library programming package.

2 INSTALLATION

The installation and operation of all three of the CIO-DIO24 series boards is very similar. Throughout this manual we use CIO-DIO24 as a generic designation for the CIO-DIO24, CIO-DIO24H, CIO-DIO24/CTR3. When required due to the differences in the boards, the specific board name is used.

The CIO-DIO24 boards are easy to use. These procedures will help you to quickly and easily setup, install, and test your board. We assume you already know how to open the PC and install expansion boards. If you are unfamiliar or uncomfortable with board installation, please refer to your computer's documentation. Though we recommend the use of InstaCal to guide you through your installation, detailed written instructions are provided in the next chapter.

We recommend you perform the software installation described in section 2.1 before installing the board in your computer.

2.1 SOFTWARE INSTALLATION

The board has a variety of switches and jumpers to set before installing the board in your computer. The simplest way to configure your board is to use the *Insta*Cal™ program provided on the CD (or floppy disk)**.**

*Insta*Cal will show you all available options, how to configure the various switches and jumpers (as applicable) to match your application requirements. It will create a configuration file that your application software (and the Universal Library) will refer to so the software you use will automatically have access to the exact configuration of the board.

Please refer to the *Extended Software Installation Manual* regarding the installation and operation of *Insta*Cal. The following hard copy information is provided as a matter of completeness, and will allow you to set the hardware configuration of the board if you do not have immediate access to *Insta*Cal and/or your computer.

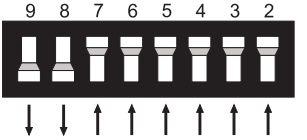
2.2 HARDWARE INSTALLATION

2.2.1 Base Address

The simplest way to set the Base address switch is by using InstaCal. The following information is provided as a reference and will be useful if you are unable to use InstaCal to guide your installation.

Each I/O board uses one or more I/O address locations within your computer's I/O address space. In order to avoid interference with other installed boards, each board must use unique addresses. The BASE ADDRESS is the board's starting location within your computer's I/O address space. Most boards will require between 2 and 16 I/O addresses. These are usually consecutive addresses above the BASE ADDRESS (e. g. Base + 1, Base + 2, ... Base + N).

The BASE ADDRESS switches are the means for setting the base address. Each switch position corresponds to one of the ISA bus address lines. By placing the switch down, the CIO-DIO24 address decode logic responds to that address bit. A complete address is constructed by entering the HEX or decimal number which corresponds to all the address bits the CIO-DIO24 will respond to. For example, in Figure 2-1 to the right, switches 9 and 8 are DOWN, all others UP.



SW	HEX
A9	200
A8	100
A7	80
A6	40
A5	20
A4	10
A3	08
A2	04

BASE ADDRESS SWITCH - Address 300H shown here.

Figure 2-1. Base Address Switches

Address 9 = 200h (512 decimal) and address 8 = 100h (256 decimal). Added together, they equal 300h (768 decimal).

NOTE !

DISREGARD THE NUMBERS PRINTED ON THE SWITCH. REFER TO THE NUMBERS PRINTED IN WHITE ON THE BOARD.

Certain address are used by the PC, others are free and may be used by the CIO-DIO24 and other expansion boards. Refer to Table 2-1.

We recommend trying BASE = 300h (768 decimal) first. This is the default address set on the boards at the factory.

2.2.2 Table of I/O Addresses

Table 2-1. P.C. I/O Addresses

HEX RANGE	FUNCTION	HEX RANGE	FUNCTION
000-00F	8237 DMA #1	2C0-2CF	EGA
020-021	8259 PIC #1	2D0-2DF	EGA
040-043	8253 TIMER	2E0-2E7	GPIB (AT)
060-063	8255 PPI (XT)	2E8-2EF	SERIAL PORT
060-064	8742 CONTROLLER (AT)	2F8-2FF	SERIAL PORT
070-071	CMOS RAM & NMI MASK (AT)	300-30F	PROTOTYPE CARD
080-08F	DMA PAGE REGISTERS	310-31F	PROTOTYPE CARD
0A0-0A1	8259 PIC #2 (AT)	320-32F	HARD DISK (XT)
0A0-0AF	NMI MASK (XT)	378-37F	PARALLEL PRINTER
0C0-0DF	8237 #2 (AT)	380-38F	SDLC
0F0-0FF	80287 NUMERIC CO-P (AT)	3A0-3AF	SDLC
1F0-1FF	HARD DISK (AT)	3B0-3BB	MDA
200-20F	GAME CONTROL	3BC-3BF	PARALLEL PRINTER
210-21F	EXPANSION UNIT (XT)	3C0-3CF	EGA
238-23B	BUS MOUSE	3D0-3DF	CGA
23C-23F	ALT BUS MOUSE	3E8-3EF	SERIAL PORT
270-27F	PARALLEL PRINTER	3F0-3F7	FLOPPY DISK
2B0-2BF	EGA	3F8-3FF	SERIAL PORT

The CIO-DIO24 BASE ADDRESS switch can be set for address in the range of 000-3FC and it should not be hard to find a free address area for your board. If you are not using IBM prototyping cards or some other board which occupies these addresses, the board's default address of 300h is free to use.

Addresses not specifically listed, such as 390 to 39F, are not reserved and may be available. Check your computer for other boards which may use I/O addresses.

2.3 INTERRUPT LEVEL SELECT

The trigger logic on the CIO-DIO24 is quite simple. Pin 1 of the 37-pin connector is an input jumper which maps the interrupt directly onto the PC bus. The signal to the bus is buffered. The buffer is enabled by a LOW level on Pin 2, interrupt enable.

Most hardware interrupts are assigned by the computer and are reserved for internal system use (refer to Table 2-2). However, some are available to the user.

Table 2-2. IRQ Assignments

NAME	DESCRIPTION	NAME	DESCRIPTION
NMI	PARITY	IRQ8	REAL TIME CLOCK
IRQ0	TIMER	IRQ9	RE-DIRECTED TO IRQ2 (AT)
IRQ1	KEYBOARD	IRQ10	NOT ASSIGNED
IRQ2	RESERVED (XT) INT 8-15 (AT)	IRQ11	NOT ASSIGNED
IRQ3	COM OR SDLC	IRQ12	NOT ASSIGNED
IRQ4	COM OR SDLC	IRQ13	NUMERIC CO-PROC.
IRQ5	HARD DISK (AT) LPT (AT)	IRQ14	HARD DISK
IRQ6	FLOPPY DISK	IRQ15	NOT ASSIGNED
IRQ7	LPT		

There is a jumper block on the CIO-DIO24 located just above the PC bus interface (Figure 2-2). The factory default setting is that no interrupt level is set. The jumper is in the 'X' position. Please leave the jumper in the 'X' position for now. Interrupts are hardware-initiated software routines. If the software you are using employs interrupt service routines, it will direct you to select an IRQ level.

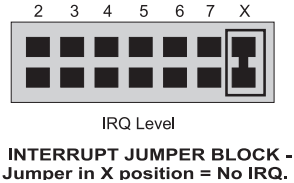


Figure 2-2. Interrupt Jumper Block

2.4 WAIT STATE JUMPER

The CIO-DIO24 boards have a wait state jumper which can enable an on-board wait state generator (Figure 2-3). A wait state is an extra delay injected into the processor's clock via the bus. This delay slows down the processor when the processor addresses the CIO-DIO24 board so that signals from slow devices (chips) will be accepted. The wait state generator on the CIO-DIO24 is only active when the CIO-DIO24 is being accessed. Your PC will not be slowed down in general by using the wait state.

Because all PC expansion board busses are slowed to either 8 MHz or 10 MHz, the wait state will generally not be required. If you experience sporadic errors from the 82C55 digital I/O chip (reset, port direction swaps), try enabling the wait state generator.

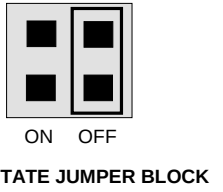


Figure 2-3. Wait State Jumper

2.5 COUNTER CLOCK SOURCE JUMPERS

The CIO-DIO24/CTR3 has a block of jumpers that allow an internal 10 MHz crystal oscillator signal to be connected to counter 0 clock input. This jumper also allows connection of the output of counter 0 to the input of counter, and connection of the output of counter 1 to the input of counter 2 (Figure 2-3), forming a 32 or 48 bit counter.

Alternately, the counters can be chained externally through the 37-pin connector. However, note that the clock for Counter 0 must come from an external source if external chaining is done.

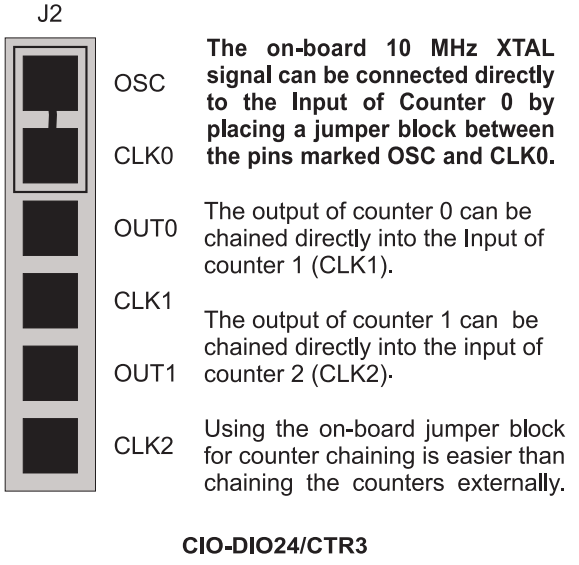

J2
OSC
CLK0
OUT0
CLK1
OUT1
CLK2
The on-board 10 MHz XTAL signal can be connected directly to the Input of Counter 0 by placing a jumper block between the pins marked OSC and CLK0.
The output of counter 0 can be chained directly into the Input of counter 1 (CLK1).
The output of counter 1 can be chained directly into the input of counter 2 (CLK2).
Using the on-board jumper block for counter chaining is easier than chaining the counters externally.
CIO-DIO24/CTR3

Figure 2-3. Counter Clock Source Jumper

3 I/ O CONNECTIONS

3.1 CABLES AND SCREW TERMINAL BOARDS

The CIO-DIO24 connector is accessible through the computer's expansion bracket. The connector is a standard 37-pin male connector. The I/O connections can be brought out to easy to use screw terminals by purchasing a C37FF-series cable and a CIO-MINI37 screw terminal accessory board. For custom cabling, a mating female connector can be purchased from Measurement Computing Corp. (part # DFCON-37) or an electronic supply outlet.

3.2 CONNECTOR DIAGRAMS

The CIO-DIO24 I/O connector is a 37-pin, D-type connector, accessible from the rear of the PC through the expansion backplate. The signals available are direct connections to the 82C55 digital I/O chip as well as the PC's internal power supplies.

The CIO-DIO24/CTR3 adds signals for an 82C54 counter chip in place of the PC power connections. The connector accepts female, 37-pin, D-type connectors such as those on the C37FF-2, a 2-foot cable with connectors available from Measurement Computing Corp.

If frequent changes to signal connections or signal conditioning is required, refer to the information on the CIO-MINI37 or CIO-SPADE50 screw terminal boards.

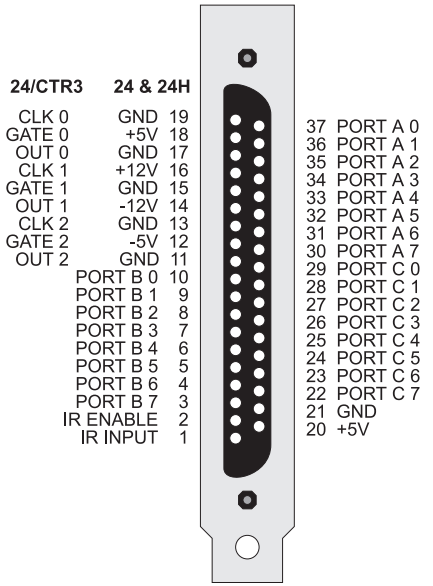


Figure 3-1. I/O Connector

3.3 SIGNAL CONNECTION CONSIDERATIONS

All the digital outputs and inputs on the CIO-DIO24 and CIO-DIO24/CTR3 connector are CMOS TTL. The CIO-DIO24H signals are buffered (high output drive) TTL.

TTL is an electronics industry term, short for Transistor Transistor Logic, which describes a standard for digital signals which are either at 0V or 5V (nominal).

The voltages and currents associated with external devices range from less than a hundred mA at a few volts for lamps etc., to 50 Amps at 220 volts for electric heaters or other high-load equipment. Attempting to connect such loads directly to the CIO-DIO24 would damage the I/O chip. Heavy loads such as these require external relays.

IMPORTANT NOTE

The 82C55 digital I/ O chip initializes all ports as inputs on power up and reset. A TTL input is a high impedance input. If you connect another TTL input device to the 82C55, it may turn ON or OFF when the 82C55 is reset. Remember, the 82C55 which is reset is in INPUT mode.

To guarantee safe output levels during startup or reset, all devices being controlled by an 82C55 should be tied high or low as required by a 2.2 Kohm resistor. Three positions (one per 8-channel port) for pull-up/pull-down resistor SIPs are provided on the board.

In addition to voltage and load matching, digital signal sources often require filtering to remove possibly hazardous electrical noise.

Please refer to *Section 6, Electronics & Interfacing*, for information on these important subjects.

4 ARCHITECTURE

4.1 82C55 CONTROL & DATA REGISTERS

Each CIO-DIO24 consists of an 82C55 parallel I/O chip (or an emulation of 82C55, mode 0, with the CIO-DIO24H). Each board uses three data and one control register and occupies four consecutive I/O locations. The CIO-DIO24/CTR3 uses four additional I/O registers for controlling the 82C54 counter chip.

The CIO-DIO24 board is easy to program with direct I/O register reads and writes. A tutorial describing how to do register programming is beyond the scope of this manual. However, it will be covered in most Introduction To Programming books.

As alternatives to register-level programming, the CIO-DIO24 is fully supported by the optional Universal Library software as well as most high-level data acquisition and control application packages (e.g. SoftWIRE™ or Labtech Notebook™). The registers and their function are summarized in Table 4-1. A more detailed description of each register is included in subsequent sections. Each register has eight bits which may be a byte of data or eight individual set/ read functions.

Table 4-1. Register Summary

ADDRESS	READ FUNCTION	WRITE FUNCTION
Base + 0	Port A Inputs of 82C55	Port A Outputs
Base + 1	Port B Inputs of 82C55	Port B Outputs
Base + 2	Port C Inputs of 82C55	Port C Outputs
Base + 3	None (n/a for 82C55)	Configure 82C55
	Added Registers for CIO-DIO24/CTR3	
Base + 4	Counter 0 (82C54)	Counter 0 Load
Base + 5	Counter 1 (82C54)	Counter 1 Load
Base + 6	Counter 2 (82C54)	Counter 2 Load
Base + 7	None	Counter Control

4.2 82C55 DIGITAL I/ O REGISTERS

Port A Data
Base Address + 0

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

Port B Data
Base Address + 1

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

Ports A & B can be programmed as input or output. Each is written to and read from in bytes, although for control and monitoring purposes, individual bits are used. Bit set/ reset and bit read functions require that unwanted bits be masked out of reads and ORed into writes.

Port C Data
Base Address + 2

7	6	5	4	3	2	1	0
C7	C6	C5	C4	C3	C2	C1	C0
CH3	CH2	CH1	CH0	CL3	CL2	CL1	CL0

Port C can be used as one, 8-bit port of either input or output, or it can be split into two, 4-bit ports which can be independently programmed to be input or output. The notation for the upper 4-bit port is CH3 to CH0, and for the lower, CL3 to CL0.

Although it can be split, every read and write to port C carries eight bits of data so unwanted information must be ANDed out of reads, and writes must be ORed with the current status of the other port.

4.2.1 Output Ports

In 82C55 mode 0 configuration, ports configured for output hold the output data written to them. This output byte can be read back by reading a port configured for output.

4.2.2 Input Ports

In 82C55 mode 0 configuration, ports configured for input read the state of the input lines at the moment the read is executed, transitions are not latched.

For information on modes 1 (strobed I/O) and 2 (bi-directional strobed I/O), you will need to acquire an Intel or AMD data book and see the 82C55 data sheet.

4.3 DIGITAL CONFIGURATION REGISTER

Base Address + 3

7	6	5	4	3	2	1	0
MS	M3	M2	A	CU	M1	B	CL
	GROUP A				GROUP B		

The 82C55 can be programmed to operate in Input/Output (mode 0), Strobed Input/ Output (mode 1) or Bi-Directional Bus (mode 2).

NOTE:

Only mode 0 is available on the CIO-DIO24H since it uses an 82C55 emulation only.

The only information included here is on programming the 82C55 in mode 0. Those wishing to use the 82C55 in modes 1 or 2, or who wish to program the 82C54 counter on the CIO-DIO24/CTR3, must procure a data book from Intel Corporation Literature Department.

When the PC is powered up or RESET, the 82C55 is reset. This places all 24 lines in Input mode. No further programming is needed to use the 24 lines as TTL inputs. To program the 82C55 for other modes, assemble the following control code into an 8-bit byte.

MS = Mode Set. 1 = mode set active

M3	M2	GROUP A FUNCTION	
0	0	Mode 0	Input/Output
0	1	Mode 1	Strobed I/O
1	X	Mode 2	Bi-directional Bus

A	B	CL	CH	Independent Function
1	1	1	1	Input
0	0	0	0	Output

M1 = 0 is mode 0 for group B. Input / Output
M1 = 1 is mode 1 for group B. Strobed Input / Output

The Ports A, B, C High, and C Low can be independently programmed for input or output.

The two groups of ports, group A and group B, may be independently programmed in one of several modes. The most commonly used is mode 0, input/output. The codes for programming the 82C55 in mode 0 (CIO-DIO24 & CIO-DIO24/CTR3) are listed in Table 4-2. The codes for programming the emulated 82C55 in mode 0, for the CIO-DIO24H, are listed in Table 4-3. NOTE: In mode 0, D7 is always “1”; D6, D5, and D2 are always “0” for all versions.

Table 4-2. 82C55 Configuration Codes - CIO-DIO24 & CIO-DIO24/CTR3 Only

D4	D3	D1	D0	HEX	DEC	A	CU	B	CL
0	0	0	0	80	128	OUT	OUT	OUT	OUT
0	0	0	1	81	129	OUT	OUT	OUT	IN
0	0	1	0	82	130	OUT	OUT	IN	OUT
0	0	1	1	83	131	OUT	OUT	IN	IN
0	1	0	0	88	136	OUT	IN	OUT	OUT
0	1	0	1	89	137	OUT	IN	OUT	IN
0	1	1	0	8A	138	OUT	IN	IN	OUT
0	1	1	1	8B	139	OUT	IN	IN	IN
1	0	0	0	90	144	IN	OUT	OUT	OUT
1	0	0	1	91	145	IN	OUT	OUT	IN
1	0	1	0	92	146	IN	OUT	IN	OUT
1	0	1	1	93	147	IN	OUT	IN	IN
1	1	0	0	98	152	IN	IN	OUT	OUT
1	1	0	1	99	153	IN	IN	OUT	IN
1	1	1	0	9A	154	IN	IN	IN	OUT
1	1	1	1	9B	155	IN	IN	IN	IN

Table 4-3. 82C55 (Emulation) Configuration Codes - CIO-DIO24H Only

D4	D3	D1	D0	HEX	DEC	A	CU	B	CL
0	0	0	0	0	0	OUT	OUT	OUT	OUT
0	0	0	1	1	1	OUT	OUT	OUT	IN
0	0	1	0	2	2	OUT	OUT	IN	OUT
0	0	1	1	3	3	OUT	OUT	IN	IN
0	1	0	0	8	8	OUT	IN	OUT	OUT
0	1	0	1	9	9	OUT	IN	OUT	IN
0	1	1	0	A	10	OUT	IN	IN	OUT
0	1	1	1	B	11	OUT	IN	IN	IN
1	0	0	0	10	16	IN	OUT	OUT	OUT
1	0	0	1	11	17	IN	OUT	OUT	IN
1	0	1	0	12	18	IN	OUT	IN	OUT
1	0	1	1	13	19	IN	OUT	IN	IN
1	1	0	0	18	24	IN	IN	OUT	OUT
1	1	0	1	19	25	IN	IN	OUT	IN
1	1	1	0	1A	26	IN	IN	IN	OUT
1	1	1	1	1B	27	IN	IN	IN	IN

4.4 82C54 COUNTER CHIP

The data sheet for the 82C54 contains programming information, input and output timing diagrams, etc. Go to Intel's web site, search for keyword "8254".

5 SPECIFICATIONS

5.1 CIO-DIO24

Power consumption

+5V:	170mA typical, 270mA max

Digital Input / Output

Digital Type	82C55
Configuration	2 banks of 8, 2 banks of 4, programmable by bank as input or output
Number of channels	24 I/O
Output High	3.0 volts min @ -2.5mA
Output Low	0.4 volts max @ 2.5mA
Input High	2.0 volts min, 5.5 volts absolute max
Input Low	0.8 volts max, -0.5 volts absolute min
Power-up / reset state	Input mode (high impedance)
Interrupts	2 through 7, jumper selectable
Interrupt enable	External (IR Enable), logic low enabled (disabled by default via internal 10k resistor to +5V)
Interrupt sources	External (IR Input), rising edge

Environmental

Operating temperature range	0 to 50°C
Storage temperature range	-40 to +100°C
Humidity	0 to 90% non-condensing

5.2 CIO-DIO24H

Power consumption

+5V:

All ports input mode	550mA typical, 700 maximum
All ports output mode, all bits low	500mA typical
All ports output mode, all bits high	360mA typical

Digital Input / Output

Digital Type	8255 mode 0 emulation
Output:	74S244
Input:	74LS373
Configuration	2 banks of 8, 2 banks of 4, programmable by bank as input or output
Number of channels	24 I/O
Output High	2.4 volts min @ -15mA

Output Low	0.5 volts max @ 64 mA
Input High	2.0 volts min, 7 volts absolute max
Input Low	0.8 volts max, -0.5 volts absolute min
Power-up / reset state	Input mode (high impedance)
Interrupts	2 through 7, jumper selectable
Interrupt enable	External (IR Enable), logic low enabled (disabled by default via internal 10k resistor to +5V)
Interrupt sources	External (IR Input), TTL, rising edge

Environmental

Operating temperature range	0 to 70°C
Storage temperature range	-40 to +100°C
Humidity	0 to 90% non-condensing

5.3 CIO-DIO24/CTR3

Power consumption

+5V:	190mA typical, 300mA max

Digital Input / Output

Digital Type	82C55
Configuration	2 banks of 8, 2 banks of 4, programmable by bank as input or output
Number of channels	24 I/O
Output High	3.0 volts min @ -2.5mA
Output Low	0.4 volts max @ 2.5mA
Input High	2.0 volts min, 5.5 volts absolute max
Input Low	0.8 volts max, -0.5 volts absolute min
Power-up / reset state	Input mode (high impedance)
Interrupts	2 through 7, jumper selectable
Interrupt enable	External (IR Enable), logic low enabled (disabled by default via internal 10k resistor to +5V)
Interrupt sources	External (IR Input), TTL, rising edge

Counter section

Counter type: 82C54

Configuration: 3 down counters, 16 bits each

Counter 0 - independent, user configurable

Source:	user connector (CLK0) and optionally, 10MHz on-board xtal oscillator, selectable by jumper
Gate:	user connector (GATE0)
Output:	user connector (OUT0) and optionally, counter 1 clock input, selectable by jumper

Counter 1 - independent, user configurable

Source:	user connector (CLK1) and optionally, counter 0 output, selectable by jumper
Gate:	user connector (GATE1)
Output:	user connector (OUT1) and optionally, counter 2 clock input, selectable by jumper

Counter 2 - independent, user configurable

Source:	user connector (CLK2) and optionally, counter 1 output, selectable by jumper
Gate:	user connector (GATE2)
Output:	user connector (OUT2)

Clock input frequency	10Mhz max
High pulse width (clock input)	30ns min
Low pulse width (clock input)	50ns min
Gate width high	50ns min
Gate width low	50ns min
Input low voltage	0.8V max
Input high voltage	2.0V min
Output low voltage	0.4V max
Output high voltage	3.0V min

Environmental

Operating temperature range	0 to 70°C
Storage temperature range	-40 to +100°C
Humidity	0 to 90% non-condensing

6 ELECTRONICS AND INTERFACING

This short introduction to the electronics most often needed by digital I/O board users covers a few key concepts.

IMPORTANT NOTE

WHENEVER THE 82C55 IS POWERED ON OR RESET, ALL PINS ARE SET TO HIGH IMPEDANCE INPUT.

The implications of this is that if you have output devices such as solid state relays, they may be switched on whenever the computer is powered on or reset. To prevent unwanted switching and to drive all outputs to a known state after power on or reset, pull all pins either high or low through a 2.2K resistor.

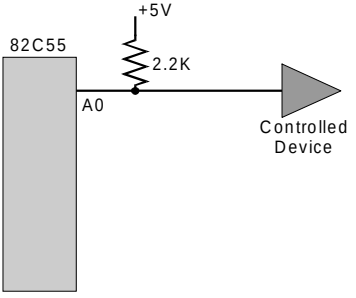
6.1 PULL UP & PULL DOWN RESISTORS

Whenever the 82C55 is powered on or reset, the control register is set to a known state. That state is mode 0, all ports input. When used as an output device to control other TTL input devices, the 82C55 applies a voltage level of near 0V for low and near 5V for high. It is the output voltage level of the 82C55 that the device being controlled responds to.

The concept of output voltage for an 82C55 in input mode is meaningless. Do not connect a volt meter to the floating input of an 82C55. It will show you nothing of meaning. In input mode the 82C55 is in 'high Z' or high impedance. If your 82C55 was connected to another input chip (the device you were controlling), the inputs of that chip are left floating whenever the 82C55 is in input mode.

If the inputs of the device you are controlling are left to float, they may float up or down. Which way they float is dependent on the characteristics of the circuit and the electrical environment and is unpredictable. This is why it often appears that the 82C55 has gone 'high' after power up. The result is that you controlled device gets turned on. That is why you need pull up/pull down resistors.

Figure 6-1 shows one 82C55 digital output with a pull-up resistor attached.



82C55 Digital Output with pull-up resistor attached

Figure 6-1. Pull-up Resistor on an 82C55

The pull-up resistor provides a reference to +5V while its value of 2200 ohms requires only 2.3 mA of drive current. If the 82C55 is reset and enters high impedance input,

the line is pulled high. At that point, both the 82C55 and the device being controlled will “see” a high signal. If the 82C55 is in output mode, the 82C55 has enough power (2.5 mA) to override the pull-up/pull down resistor's high signal and drive the line to 0 volts. If the 82C55 asserts a high signal, the pull up resistor guarantees that the line goes to +5V.

A pull-down resistor accomplishes the same task except that the line is pulled low when the 82C55 is reset. The 82C55 has more than enough power to drive the line high.

CIO-DIO24 series boards have positions for three SIPs (pull-up/pull-down resistors in Single Inline Packages). The positions are marked A, B and C and are located around the periphery of the 82C55 chip (except on the CIO-DIO24H, they are adjacent to U12, 13 and 14).

A 2.2K, eight-resistor SIP has all eight resistors connected at one end to a single common point. The other ends connect to eight pins on the SIP. The common pin is marked with a dot and is at one end of the SIP.

The SIP may be installed as pull-up or pull-down. At each location, A, B & C on the CIO-DIO24 series boards, there are 10 holes in a line. One end of the line is +5V (marked “HI”). The other end is at GND (marked “LO”). The eight holes in the middle are connected to the eight lines of a port, either A, B, or C.

For a “pull-up” function, install the SIP with pin one (the marked end with the common connection mentioned above) toward the HI location. Install the SIP with the common pin toward LO for a “pull-down” function.

A resistor value of 2.2K is recommended. Use different values only if you have calculated the necessity of doing so.

NOTE: UNCONNECTED INPUTS FLOAT.

Keep in mind that unconnected inputs float. If you are using the CIO-DIO24 board for input, and have unconnected inputs, ignore the data from those lines.

In other words, if you connect to bit A0 and not bit A1, do not be surprised if A1 stays low, stays high or may even track A0. It is unconnected and thus, unspecified. The 82C55 is not malfunctioning.

You do not have to tie input lines, and unconnected lines will not affect the performance of connected lines. Just make sure that you mask out any unconnected bits in software.

6.2 TTL TO SOLID STATE RELAYS

Many applications require digital outputs to switch AC and DC voltage motors on and off and to monitor AC and DC voltages. These AC and high DC voltages cannot be controlled or read directly by the TTL digital lines of a CIO-DIO24.

Solid State Relays, such as those available from Measurement Computing Corp. allow control and monitoring of AC and high DC voltages and provide 750V isolation. Solid State Relays (SSRs) are the recommended method of interfacing to AC and high DC signals.

The most convenient way to use solid state relays and a CIO-DIO24 board is to purchase a Solid State Relay Rack (SSR). An SSR Rack is a circuit board with output buffers which supply enough power to switch the SSRs. SSRs are socketed. SSR Racks are available from Measurement Computing Corp.

The high current outputs of the CIO-DIO24H boards are suitable to drive SSRs directly but the CMOS outputs of the CIO-DIO24 and CIO-DIO24/CTR3 do not have sufficient drive to connect directly to most SSRs. If you only want to drive one or two SSRs with CMOS outputs, all you need is a 74S244 output buffer chip between the 82C55 output and the SSR. The SSR will need 5 Volt power also.

6.3 VOLTAGE DIVIDERS

An alternative method of measuring a signal which varies over a range greater than the input range of a digital input is to use a voltage divider. When correctly designed, it can drop the voltage of the input signal to a safe level the digital input can accept.

Ohm's law states:

> Voltage = Current x Resistance

Kirkoff's voltage law states:

> The sum of the voltage drops around a circuit will be equal to the voltage drop for the entire circuit.

In a voltage divider, the voltage across one resistor in a series circuit is proportional to the total resistance divided by the one resistor (see formula below).

The object in a voltage divider is to choose two resistors having the proportions of the maximum voltage of the input signal to the maximum allowed input voltage.

The formula for attenuation is:

$$\text{Attenuation} = \frac{R1 + R2}{R2}$$

$$2 = \frac{10K + 10K}{10K}$$

For example, if the signal varies between 0 and 20 volts and you wish to measure that with an analog input with a full scale range of 0 to 10 volts, the attenuation (A) is 2:1 or just 2.

R1 = (A-1) x R2 For a given attenuation, pick a resistor and call it R2, the use this formula to calculate R1.

Digital inputs often require the use of voltage dividers. For example, if you wish to measure a digital signal that is at 0 volts when off and 24 volts when on, you cannot connect that directly to a digital input. The voltage must be dropped to 5 volts max when on. The attenuation is 24:5 or 4.8.

Using the equation above, if R2 is 1K, R1 = (4.8–1) x 1000 = 3.8K.

Remember that a TTL input is 'on' when the input voltage is greater than 2.5 volts.

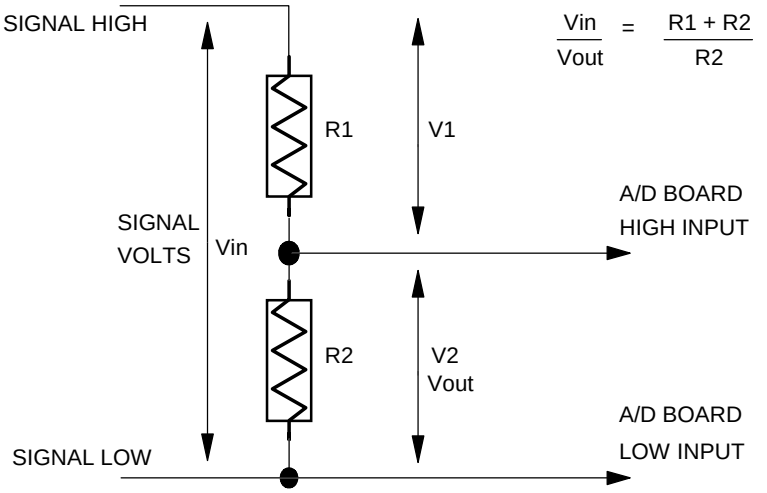


Figure 6-2. Voltage Divider Theory

NOTE The resistors, R1 and R2, are going to dissipate power in the divider circuit according to the equation $W = I^2 \times R$; (Current (I) = Voltage/Resistance). The higher the value of the resistance (R1 + R2), the less power dissipated by the divider circuit. Here is a simple rule:

For attenuation of <5:1, no resistor should be less than 10K.

For attenuation of > 5:1, no resistor should be less than 1K.

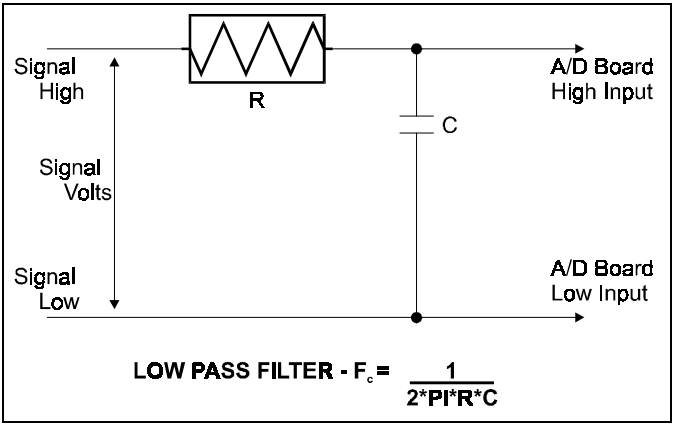
6.4 LOW PASS FILTER TO DE-BOUNCE INPUTS

A low pass filter can be placed on the signal input between a signal source and a DIO board. It prevents frequencies greater than the cut-off frequency from entering the board's digital inputs.

The cut-off frequency is that frequency above which little variation of voltage with respect to time may enter the circuit. For example, if a low-pass filter had a cut-off frequency of 30 Hz, interference associated with line voltage (60 Hz) would be mostly filtered out but a signal of 25 Hz would pass with less attenuation.

Also, in a digital circuit, a low-pass filter is often used to remove contact bounce noise signals from a switch or a relay contacts. Also, in a digital circuit, a low-pass filter might be used to “de-bounce” (filter) an input from a switch or external relay.

Unless switch/relay contacts are mercury-wetted, they tend to bounce briefly on closure, generating a pulsating noise signal. This can easily lead to erroneous counts unless filtered out.



A simple low-pass filter can be constructed from one resistor (R) and one capacitor (C). The cut-off frequency is determined according to the formula:

$$Fc = \frac{1}{2 \pi R C}$$

$$R = \frac{1}{2 \pi C Fc}$$

Where π= 3.14...
R = ohms
C = Farads
Fc = cut-off frequency in cycles/second.

For Your Notes

EC Declaration of Conformity

We, Measurement Computing Corporation, declare under sole responsibility that the product:

Part Number	Description
CIO-DIO24	Digital I/O board for ISA bus.
CIO-DIO24H	Digital I/O board for ISA bus.
CIO-DIO24/CTR3	DIO/Counter board for ISA bus.

to which this declaration relates, meets the essential requirements, is in conformity with, and CE marking has been applied according to the relevant EC Directives listed below using the relevant section of the following EC standards and other normative documents:

EU EMC Directive 89/336/EEC: Essential requirements relating to electromagnetic compatibility.

EU 55022 Class B: Limits and methods of measurements of radio interference characteristics of information technology equipment.

EN 50082-1: EC generic immunity requirements.

IEC 801-2: Electrostatic discharge requirements for industrial process measurement and control equipment.

IEC 801-3: Radiated electromagnetic field requirements for industrial process measurements and control equipment.

IEC 801-4: Electrically fast transients for industrial process measurement and control equipment.

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